Priyajit Mukherjee

Curriculum Vitae

Contact Information

Basic Engineering Department,
Government College of Engineering & Textile Technology Serampore,
West Bengal, India.

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About

Presently, I am an Assistant Professor in Electronics and Communication Engineering, at Government College of Engineering & Textile Technology Serampore.

Education

2013–2018 **Doctor of Philosophy**, *Indian Institute of Technology*, Kharagpur.
Strategies for Thermal-Aware Application Specific and Regular Network-on-Chip Design.

2011–2013 **Master of Technology**, *Indian Institute of Engineering Science and Technology, Shibpur*, Howrah, *Aggregate – 89.27%*.
VLSI Design

2007–2011 **Bachelor of Technology**, *West Bengal University of Technology*, *DGPA – 9.11*.
Electronics and Communication Engineering

2007 **Higher Secondary**, *West Bengal Council of Higher Secondary Education (WBCHSE)*, *Aggregate – 83.6%*.

2005 **Secondary**, *West Bengal Board of Secondary Education (WBBSE)*, *Aggregate – 82.87%*.

PhD Dissertation

Title *Strategies for Thermal-Aware Application Specific and Regular Network-on-Chip Design*

Supervisors Professor Santanu Chattopadhyay

Description This dissertation contributes towards the thermal-aware application specific and regular 2D and 3D Network-on-Chip design. Specifically the thesis addresses - White Space Redistribution in Core and Router Placement in ASNoCs, Path Synthesis, Task Allocation and Scheduling, and Routing in 3D Mesh NoCs.

Masters Thesis

Title *Broadcast Enabled Photonic Network-on-Chip for Many Core Processors*

Description In this work, both Code Division Multiplexing (CDMA) and Wave Division Multiplexing (WDM) have been used to design a broadcast enabled Photonic NoC. ASIC Designs of the CDMA Transmitter and Receiver Units have been performed.

B.Tech Project

Title *Blind Calculator*

Description In this work, we have developed a hands free calculator using a speech recognition IC, HM2007 and microcontroller 89C51.

Research Interests

- Application-specific Network-on-Chip (NoC) synthesis
- Thermal-aware Routing Techniques in 3D NoCs
- Power and Thermal aware Task Scheduling in MPSoCs
- FPGA and ASIC based Digital System Design (DSD)
- Application of Evolutionary Algorithms (eg. PSO, SA, GA etc.) in different Phases of DSD

Technical skills

Programming Languages	C, C++, VHDL, Verilog, Shell Scripting.
Software and Tools	Xilinx ISE, Synopsys Design Vision, Keil uVision, Arduino, Cadence Virtuoso, Mentor ModelSim, MATLAB, OMNET++, Noxim, BookSim, Orion, TGFF, HotSpot, Access Noxim, SniperSim, Tanner EDA.

Computer skills

Basic	Linux
Intermediate	LaTeX, Microsoft Office, Microsoft Windows

Publications

Journals

J6 **Priyajit Mukherjee** and Santanu Chattopadhyay, "Low Power Low Latency Floorplan-aware Path Synthesis in Application-Specific Network-on-Chip Design," *Elsevier Integration, the VLSI Journal*, Volume 58, 2017, Pages 167-188, ISSN 0167-9260, http://dx.doi.org/10.1016/j.vlsi.2017.02.010.

J5 Navonil Chatterjee, Suraj Paul, **Priyajit Mukherjee**, and Santanu Chattopadhyay, "Deadline and energy aware dynamic task mapping and scheduling for Network-on-Chip based multi-core platform," *Elsevier Journal of Systems Architecture*, Volume 74, 2017, Pages 61-77, ISSN 1383-7621, http://dx.doi.org/10.1016/j.sysarc.2017.01.008.

J4 **Priyajit Mukherjee**, Sandeep D'Souza, and Santanu Chattopadhyay, "Area Constrained Performance Optimized ASNoC Synthesis with Thermal-aware White Space Allocation and Redistribution," *Elsevier Integration, the VLSI Journal*, Volume 60, 2018, Pages 167-189, ISSN 0167-9260,https://doi.org/10.1016/j.vlsi.2017.09.004.

J3 Kanchan Manna, **Priyajit Mukherjee**, Santanu Chattopadhyay, and Indranil Sengupta, "Thermal-Aware Application Mapping Strategy for Network-on-Chip Based System Design," *IEEE Transaction on Computers*, Volume. 67, no. 4, 2018, Pages. 528-542, doi: 10.1109/TC.2017.2770130

J2 N Prasad, **Priyajit Mukherjee**, Santanu Chattopadhyay, and Indrajit Chakrabarti, "Design and evaluation of ZMesh topology for on-chip interconnection networks," *Elsevier Journal of Parallel and Distributed Computing*, Volume 113, 2018, Pages 17-36, ISSN 0743-7315, https://doi.org/10.1016/j.jpdc.2017.10.011.

J1 Navonil Chatterjee, **Priyajit Mukherjee**, and Santanu Chattopadhyay, "Reliability Aware Application Mapping onto Mesh based Network-on-Chip," *Elsevier Integration, the VLSI Journal*, Feb 2018, DOI10.1016/j.vlsi.2018.02.002.

Conferences

C5 **Priyajit Mukherjee** and Santanu Chattopadhyay, "An ILP-based floorplan-aware path synthesis technique for Application-Specific NoC design," in *2016 3rd International Conference on Recent Advances in Information Technology (RAIT)*, Dhanbad, 2016, pp. 543-548, doi: 10.1109/RAIT.2016.7507959

C4 Soumyajit Poddar, Prasun Ghosal, **Priyajit Mukherjee**, Suman Samui and Hafizur Rahaman, "An Area and Power Efficient Dynamic TDMA Based Photonic Network on Chip," *2013 International Symposium on Electronic System Design*, Singapore, 2013, pp. 113-117. doi: 10.1109/ISED.2013.29

C3 Soumyajit Poddar, Prasun Ghosal, **Priyajit Mukherjee**, Suman Samui and Hafizur Rahaman, "Design of an NoC with on-chip photonic interconnects using adaptive CDMA links," *2012 IEEE International SOC Conference*, Niagara Falls, NY, 2012, pp. 352-357. doi: 10.1109/SOCC.2012.6398331

C2 Soumyajit Poddar, Prasun Ghosal, **Priyajit Mukherjee**, Suman Samui, Hafizur Rahaman, "A photonic network on chip with CDMA links", *in 16th international conference on Progress in VLSI Design and Test (VDAT)*, Shibpur, July 2012, DOI:10.1007/978-3-642-31494-0_50.

C1 Navonil Chatterjee, **Priyajit Mukherjee**, Santanu Chattopadhyay, "A strategy for fault tolerant reconfigurable Network-on-Chip design", *in 20th international Symposium on VLSI Design and Test (VDAT)*, Guwahati, 2016, pp. 1-2. doi: 10.1109/ISVDAT.2016.8064893.

Awards and Achievements

2014 Feb. Secured first position in M.Tech and awarded silver medal from the Governor of West Bengal.

GATE Qualified EC in 2011